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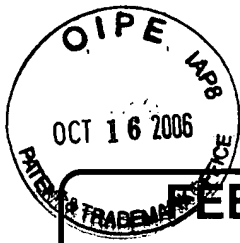
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| <b>TRANSMITTAL FORM</b><br><i>(to be used for all correspondence after initial filing)</i> |    | Application No.        | 10/677,039         |
|                                                                                            |    | Filing Date            | September 30, 2003 |
|                                                                                            |    | First Named Inventor   | Nicholas G. Samra  |
|                                                                                            |    | Art Unit               | 2183               |
|                                                                                            |    | Examiner Name          | Johnson, Brian P.  |
| Total Number of Pages in This Submission                                                   | 27 | Attorney Docket Number | 42P17033           |

| ENCLOSURES (check all that apply)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
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| <input checked="" type="checkbox"/> Fee Transmittal Form<br><br><input checked="" type="checkbox"/> Fee Attached<br><br><input type="checkbox"/> Amendment / Response<br><br><input type="checkbox"/> After Final<br><input type="checkbox"/> Affidavits/declaration(s)<br><br><input type="checkbox"/> Extension of Time Request<br><br><input type="checkbox"/> Express Abandonment Request<br><br><input type="checkbox"/> Information Disclosure Statement<br><br><input type="checkbox"/> PTO/SB/08<br><br><input type="checkbox"/> Certified Copy of Priority Document(s)<br><br><input type="checkbox"/> Response to Missing Parts/Incomplete Application<br><br><input type="checkbox"/> Basic Filing Fee<br><input type="checkbox"/> Declaration/POA<br><br><input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53 | <input type="checkbox"/> Drawing(s)<br><br><input type="checkbox"/> Licensing-related Papers<br><br><input type="checkbox"/> Petition<br><br><input type="checkbox"/> Petition to Convert a Provisional Application<br><br><input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address<br><br><input type="checkbox"/> Terminal Disclaimer<br><br><input type="checkbox"/> Request for Refund<br><br><input type="checkbox"/> CD, Number of CD(s)<br><input type="checkbox"/> Landscape Table on CD | <input type="checkbox"/> After Allowance Communication to TC<br><br><input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences<br><br><input checked="" type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)<br><br><input type="checkbox"/> Proprietary Information<br><br><input type="checkbox"/> Status Letter<br><br><input checked="" type="checkbox"/> Other Enclosure(s) (please identify below):<br><div style="border: 1px solid black; padding: 5px; margin-top: 5px;">-return receipt postcard</div> |
| Remarks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

| SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT |                                                                                          |
|--------------------------------------------|------------------------------------------------------------------------------------------|
| Firm or Individual name                    | Jonathan S. Miller, Reg. No. 48,534<br><b>BLAKELY, SOKOLOFF, TAYLOR &amp; ZAFMAN LLP</b> |
| Signature                                  |                                                                                          |
| Date                                       | October 11, 2006                                                                         |

| CERTIFICATE OF MAILING/TRANSMISSION                                                                                                                                                                                                                                                                     |                   |      |                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------|------------------|
| I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. |                   |      |                  |
| Typed or printed name                                                                                                                                                                                                                                                                                   | Amber D. Saunders |      |                  |
| Signature                                                                                                                                                                                                                                                                                               |                   | Date | October 11, 2006 |

Based on PTO/SB/21 (09-04) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 11/30/2005.  
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# FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

## Complete if Known

Application Number 10/677,039  
Filing Date September 30, 2003  
First Named Inventor Nicholas G. Samra  
Examiner Name Johnson, Brian P.  
Art Unit 2183  
Attorney Docket No. 42P17033

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT (\$) 500.00

## METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify):

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee  
☒ Charge any additional fee(s) or underpayment of fee(s) ☒ Credit any overpayments  
under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

## FEE CALCULATION

### 1. EXTRA CLAIM FEES

|                    | Extra Claims | Fee from below | Fee Paid |
|--------------------|--------------|----------------|----------|
| Total Claims       | 28           | 50.00          | \$0.00   |
| Independent Claims | 3            | 200.00         | \$0.00   |
| Multiple Dependent |              |                |          |

| Large Entity |          | Small Entity |          | Fee Description                                           |
|--------------|----------|--------------|----------|-----------------------------------------------------------|
| Fee Code     | Fee (\$) | Fee Code     | Fee (\$) |                                                           |
| 1202         | 50       | 2202         | 25       | Claims in excess of 20                                    |
| 1201         | 200      | 2201         | 100      | Independent claims in excess of 3                         |
| 1203         | 360      | 2203         | 180      | Multiple Dependent claim, if not paid                     |
| 1204         | 790      | 2204         | 395      | **Reissue independent claims over original patent         |
| 1205         | 300      | 2205         | 150      | **Reissue claims in excess of 20 and over original patent |
| SUBTOTAL (1) |          | (\$)         |          | 0.00                                                      |

\*\*or number previously paid, if greater, For Reissues, see below

### 2. ADDITIONAL FEES

| Large Entity        |          | Small Entity |          | Fee Description                                                  | Fee Paid |
|---------------------|----------|--------------|----------|------------------------------------------------------------------|----------|
| Fee Code            | Fee (\$) | Fee Code     | Fee (\$) |                                                                  |          |
| 1051                | 130      | 2051         | 65       | Surcharge - late filing fee or oath                              |          |
| 1052                | 50       | 2052         | 25       | Surcharge - late provisional filing fee or cover sheet.          |          |
| 2053                | 130      | 2053         | 130      | Non-English specification                                        |          |
| 1251                | 120      | 2251         | 60       | Extension for reply within first month                           |          |
| 1252                | 450      | 2252         | 225      | Extension for reply within second month                          |          |
| 1253                | 1,020    | 2253         | 510      | Extension for reply within third month                           |          |
| 1254                | 1,590    | 2254         | 795      | Extension for reply within fourth month                          |          |
| 1255                | 2,160    | 2255         | 1,080    | Extension for reply within fifth month                           |          |
| 1401                | 500      | 2401         | 250      | Notice of Appeal                                                 |          |
| 1402                | 500      | 2402         | 250      | Filing a brief in support of an appeal                           | 500.00   |
| 1403                | 1,000    | 2403         | 500      | Request for oral hearing                                         |          |
| 1451                | 1,510    | 2451         | 1,510    | Petition to institute a public use proceeding                    |          |
| 1460                | 130      | 2460         | 130      | Petitions to the Commissioner                                    |          |
| 1807                | 50       | 1807         | 50       | Processing fee under 37 CFR 1.17(q)                              |          |
| 1806                | 180      | 1806         | 180      | Submission of Information Disclosure Stmt                        |          |
| 1809                | 790      | 1809         | 395      | Filing a submission after final rejection (37 CFR § 1.129(a))    |          |
| 1810                | 790      | 2810         | 395      | For each additional invention to be examined (37 CFR § 1.129(b)) |          |
| Other fee (specify) |          |              |          |                                                                  |          |
| SUBTOTAL (2)        |          | (\$)         |          |                                                                  | 500.00   |

## SUBMITTED BY

Complete (if applicable)

Name (Print/Type) Jonathan S. Miller Registration No. 48,534 Telephone (310) 207-3800  
Signature [Signature] Date 10/14/06



Attorney's Docket No. 42390P17033

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application for:

**Nicholas G. Samra, et al.**

Serial No. 10/677,039

Filed: September 30, 2003

For: Flag Value Renaming

Examiner: Johnson, Brian

Art Unit: 2183

Confirmation No. 7715

Assistant Commissioner for Patents  
Board of Patent Appeals and Interferences  
P.O. Box 1450  
Alexandria, VA 22313-1450

**APPEAL BRIEF**

Pursuant to 37 C.F.R. § 41.37, Appellants submit the following Appeal Brief for consideration by the Board of Patent Appeals and Interferences ("Board"). Appellants also submit herewith a check in the amount of \$500.00 to cover the cost of filing this appeal brief, as set forth in 37 C.F.R. § 41.20(b)(2). Please charge any additional amounts due or credit any overpayment to Deposit Account No. 02-2666.

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## **I. REAL PARTY IN INTEREST**

Nicholas G. Samra, et al., the parties named in the caption, transferred their rights in the subject application through an assignment recorded on reel/frame 015003/0150 on February 24, 2004 to Intel Corporation of Santa Clara, California. Accordingly, Intel Corporation is the real party in interest.

## **II. RELATED APPEALS AND INTERFERENCES**

There are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

## **III. STATUS OF CLAIMS**

Claims 1-28 are pending in this application. All claims stand rejected. Appellants seek review of claims 1-28.

## **IV. STATUS OF AMENDMENTS**

No amendments were submitted after the Final Office Action mailed May 31, 2006.

## **V. SUMMARY OF CLAIMED SUBJECT MATTER**

The claimed subject matter relates to renaming flag registers (paragraph 12). Three independent claims (claims 1, 9, and 19) and twenty-five dependent claims (claims 2-8, 10-18, and 20-28) are presented in this appeal.

Flag value renaming is a mechanism that allows for the tracking of flag values (paragraph 13). Flag values may be set or cleared by either an instruction that writes a value directly to the

flag register (a direct write), or by data that is obtained from the data path of the machine (an indirect write) (paragraph 13). A direct update instruction can directly set or clear the appropriate flag (paragraph 14). A direct update instruction is effectively executed by storing the updated flag value in a renamer at rename time, that is, before retirement of the instruction (paragraph 17). Thus, a succeeding instruction can access the updated flag value before the completion of the direct update instruction (paragraph 22).

An indirect update instruction reads data from the system data path and updates a flag value based upon that data (paragraph 15). An indirect update instruction does not update values until retirement (paragraph 27). Thus, a succeeding instruction does not know the updated flag value until after the completion of the indirect update instruction (paragraph 22).

Independent claim 1 is a method, which sets a flag for a processor via a first instruction. The first instruction is either a direct update instruction or an indirect update instruction (paragraph 13). If the flag is set by a direct update instruction, a succeeding second instruction that reads the flag is executed before the completion of the first instruction (paragraph 22). If the flag is set by an indirect update instruction, the second instruction is delayed until after the completion of the first instruction (paragraph 30).

Dependent claim 2 modifies the method of claim 1 to further include, if the first instruction is a direct update instruction, storing a value for the flag in a renamer (paragraph 17).

Dependent claim 3 modifies the method of claim 2 to further include, if the first instruction is an indirect update instruction, storing a value in a buffer and storing the value in the renamer upon retirement of the indirect update instruction (paragraph 18).

Dependent claim 4 modifies the method of claim 3 to further include checking the value of a register scoreboard prior to accessing the flag (paragraph 25).

Dependent claim 5 modifies the method of claim 4 to further include, if the first instruction is an indirect update instruction, setting the register scoreboard prior to storing the value in the renamer and clearing the register scoreboard after storing the value in the renamer (paragraph 18).

Dependent claim 6 modifies the method of claim 1 to further include storing the value for the flag in shadow logic (paragraph 19).

Dependent claim 7 modifies the method of claim 6 to further include that the shadow logic is enabled if the value was provided by a direct update instruction (paragraph 19).

Dependent claim 8 modifies the method of claim 7 to further include that the shadow logic is disabled if the value was not provided by a direct update instruction (paragraph 19).

Independent claim 9 recites a processor, which includes an execution unit to execute instructions and a renamer (paragraph 30). The renamer renames a flag register and stores the value for the flag register (paragraph 17). The value of the flag register is set by one of a plurality of processes (paragraph 13). The processes include directly setting the flag register by a first instruction or setting the flag register to a data value obtained by a second instruction (paragraph 22). If the value of the flag register is set by the first instruction, a succeeding third instruction is executed without being stalled (paragraph 22). If the value of the flag register is set by the second instruction, the third instruction is stalled until conclusion of the second instruction (paragraph 22).

Dependent claim 10 modifies the processor of claim 9 to further include a scoreboard register (paragraph 16). The first instruction and the second instruction checking the scoreboard register before setting the flag register (paragraph 16).

Dependent claim 11 modifies the processor of claim 10 to further include that the first instruction and the second instruction delay storage of the flag register if the scoreboard register is enabled (paragraph 16).

Dependent claim 12 modifies the processor of claim 11 to further include that the execution of the second instruction includes setting the scoreboard register before setting the flag register and clearing the scoreboard register after setting the flag register (paragraph 18).

Dependent claim 13 modifies the processor of claim 9 to further include shadow logic to store values for the flag register (paragraph 19).

Dependent claim 14 modifies the processor of claim 13 to further include that the shadow logic includes a validity register to indicate validity of stored values for the flag register (paragraph 19).

Dependent claim 15 modifies the processor of claim 14 to further include that the validity register is enabled if a value for the flag register is provided by the first instruction and the validity register is disabled if the value for the flag register is provided by the second instruction (paragraph 19).

Dependent claim 16 modifies the processor of claim 9 to further include that the flag register is one of an interrupt flag or a direction flag (paragraph 14).

Dependent claim 17 modifies the processor of claim 16 to further include that the first instruction is an instruction to set or clear the flag register (paragraph 13).

Dependent claim 18 modifies the processor of claim 9 to further include that the second instruction is an instruction to pop a data value from a memory stack (paragraph 15).

Independent claim 19 is a system, which includes a bus, a flash memory coupled to the bus, and a processor coupled to the bus (paragraphs 31-35). The processor comprises an execution unit to execute instructions (paragraph 31). The processor also comprises a renamer that renames a flag register and stores the value for the flag register (paragraph 17). The value of the flag register is set by one of a plurality of processes (paragraph 13). The processes include directly setting the flag register by a first instruction or setting the flag register to a data value obtained by a second instruction (paragraph 22). A succeeding third instruction is executed without being stalled if the value of the flag register is set by the first instruction (paragraph 22). The third instruction is stalled until conclusion of the second instruction if the value of the flag register is set by the second instruction (paragraph 22).

Dependent claims 20-28 modify the system of claim 19 to further include elements corresponding to the elements of claims 10-18, respectively.

## **VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

Claims 1-3, 6-9, and 13-15 stand rejected under 35 USC § 102(b) as allegedly being anticipated by U.S. Patent No. 5,632,023 issued to White et al. (hereinafter “White”).

Claims 4, 5, 10-12, and 20-22 stand rejected under 35 U.S.C. § 103 as allegedly being unpatentable over White in view of “Computer Architecture a Quantitative Approach” by Patterson, D.A., Hennessy, J.L., 2nd edition, 1996 Morgan Kauffmann Publishers, Inc., pages 242-247, (hereinafter “Hennessy”).

Claims 16-19 and 23-28 stand rejected under 35 U.S.C. § 103 as being allegedly unpatentable over White.

## **VII. ARGUMENT**

The Examiner has rejected claims 1-3, 6-9, and 13-15 under 35 U.S.C. §102 over White, claims 4, 5, 10-12, and 20-22 under 35 U.S.C. §103(a) over White in view of Hennessy, and claims 16-19 and 23-28 under 35 U.S.C. §103(a) over White.

All of the claims do not stand or fall together. The basis for the separate patentability of the claims is set forth below.

### **A. Overview of Cited References**

#### **1. U.S. Patent No. 5,632,023 issued to White**

White discloses a superscalar microprocessor that includes a reorder buffer for implementing register renaming (abstract). A first instruction generates a result value that is to be stored in a destination register. The result value is assigned a location in the reorder buffer and is associated with a destination register number (col. 4, lines 46-48). If the result value has not yet been computed, a tag for the result value is stored in the assigned location (col. 4, lines 57-58). When a second instruction in the instruction stream refers to the destination register number, the second instruction obtains either the result value stored in the reorder buffer or the tag for this value (col. 4, lines 53-58).

When a branch instruction is decoded, the decoder informs the reorder buffer that this instruction must have access to a flag (hereinafter, “the requested flag”) (col. 33, lines 26-30). The reorder buffer scans the entries of its flag operand storage area for the most recent update to the flag sub-group associated with the requested flag (col. 33, lines 45-47 and FIG. 11, feature 515). A test is conducted to determine if a dependency exists with respect to the requested flag (col. 33, lines 48-40 and FIG. 11, feature 520). If it is determined that no dependency exists with

respect to the requested flag, the contents of the flag register are transmitted to a branch function unit (col. 34, lines 46-50 and FIG. 11, feature 545). If it is determined that the dependencies with respect to the requested flag sub-group have been resolved, the reorder buffer transmits the requested flag sub-group to the branch functional unit (FIG. 11, feature 540). If there is an unresolved dependency with respect to the requested flag sub-group, a flag tag is sent to the branch functional unit instead of the actual flag values (col. 34, lines 6-17 and FIG. 11, feature 525). Thus, the branch instruction obtains the requested flag value if no unresolved dependency exists with respect to the requested flag sub-group in all of the reorder buffer entries.

White does not disclose a direct update instruction that sets a flag value. Further, White does not disclose that the execution of a succeeding instruction depends on whether the prior instruction is a direct update instruction or an indirect update instruction.

## 2. “Computer Architecture a Quantitative Approach” by Hennessy

Hennessy is relied on for disclosing a scoreboarding technique that allows instructions to be executed out of order. Hennessy discloses the use of a scoreboard to track data dependencies for read/write operations. However, Hennessy does not disclose a direct update instruction that sets a flag value. Hennessy also does not disclose that the execution of a succeeding instruction depends on whether the prior instruction is a direct update instruction or an indirect update instruction.

### **B. Claims Rejected Under 35 U.S.C. § 102(b) Over White**

Claims 1-3, 6-9, and 13-15 stand rejected under 35 USC § 102(b) as allegedly being anticipated by White. Appellants submit that White does not teach each of the elements of these claims.

Claims 1-3, 6-9, and 13-15

Claim 1 include the elements of “the first instruction being either a direct update instruction or an indirect update instruction” and “if the setting of the flag is by a direct update instruction, executing a succeeding second instruction that reads the flag prior to completion of the first instruction.” Appellants submit that White does not teach the direct update instruction, and thus does not teach flag renaming and handling if the first instruction is a direct update instruction.

According to White, when a conditional branch is encountered, a reorder buffer is scanned to identify dependencies between the flag values to be read by the conditional branch and the prior flag updating instructions stored in the reorder buffer (FIG. 11). A dependency check is performed at block 520 of FIG. 11 for the conditional branch. A “no dependency” path, a “resolved dependency” path, and an “unresolved dependency” path are shown to flow from block 520 after the conditional branch is decoded.

The Examiner applies an alleged “broadest reasonable definition” to the claimed term “direct update instruction” and “indirect update instruction,” because it is alleged that there is no definition of these terms in either the specification or claims (page 14 of Final Office Action). However, Appellants submit that these terms are defined in the specification. The specification clearly discloses that a direct update instruction is an instruction that can directly set or clear the appropriate flag (paragraph 14 of specification). The specification also clearly discloses that an indirect update instruction is an instruction that reads data from the system data path and updates a flag value based upon that data (paragraph 15 of specification). The disclosed meaning of the terms is consistent with their plain meaning, which is an instruction that directly updates a value

and an instruction that indirectly updates a value, respectively. Thus, the terms are disclosed in the specification and are understandable by their plain meaning.

The “broadest reasonable definition” used by Examiner is that the direct and the indirect update instructions are equivalent to when no dependency exists and when the update depends on a prior instruction, respectively, as disclosed by White (page 14 of Final Office Action).

However, when there is no dependency between a branch instruction and any of the prior instructions in the reorder buffer, none of the instructions, including the branch instruction and the buffered prior instructions, is a direct update instruction.

With respect to the branch instruction, the Examiner indicates that “nothing in the present claims limits the cited ‘first’ or ‘second’ instructions to being non-branch instructions” (page 14 of Final Office Action). However, a conditional branch is an instruction that branches conditionally depending on the value of a flag (e.g., JO “jump on overflow”). A conditional branch reads a flag and reacts to the value of the flag. Thus, when there is no dependency, the branch instruction does not directly update the flag value but instead directly reads the flag value. Thus, the branch instruction cannot be a direct update instruction.

With respect to the buffered prior instructions, White does not disclose that any of the prior instructions is a direct update instruction within the plain meaning of terms and according to Appellants’ specification. Even assuming, for the sake of argument, that a direct update instruction is defined as alleged by the Examiner, the definition would lead to the same prior instruction being a direct update with respect to one branch instruction and an indirect update with respect to another branch instruction. This is because dependency is relative to the branch instruction and does not distinguish the type of a prior instruction as being direct or indirect.

Thus, White does not teach a direct update instruction and does not teach flag renaming and handling if the first instruction is a direct update instruction.

The examples in White disclose at most indirect update instructions, e.g., integer operations that produce results causing flag values to be updated (e.g., col. 29, lines 17-19, 31-32, FIG. 10). Thus, the dependency check of block 520 is performed in the context of indirect update instructions that are decoded prior to a conditional branching instruction. The Examiner recognizes this point by stating “it is explicitly written that instruction, considered to be an indirect update instruction does, in fact, update the flag register” (see the Advisory Action). Thus, White at most discloses that an instruction preceding the conditional branch is an indirect update instruction. Thus, there is nothing in White that discloses a direct update instruction.

Moreover, the Examiner has misinterpreted the claim as not necessarily including the direct update instruction (see the Advisory Action). The Examiner bases his interpretation on the element of “the first instruction being either a direct update instruction or an indirect update instruction.” However, the Examiner clearly overlooks the positive limitations of claim 1, which include “if the setting of the flag is by a direct update instruction, executing a succeeding second instruction that reads the flag prior to completion of the first instruction.” Thus, to show that White teaches each of the elements of claim 1, the Examiner must identify the condition of a flag being set by a direct update instruction and the operation that follows the condition.

In the Advisory Action, the Examiner further asserts that “for Applicant to fully overcome the rejection, Applicant is required to show BOTH the direct update instruction AND the indirect update instruction are not disclosed in the reference.” The law requires the Examiner to bear the burden of proving anticipation. Until the Examiner satisfies the burden of proof, Appellants are not required to show why the prior art does not show each of the claimed

elements. As mentioned above, the Examiner has not shown that White discloses the direct update instruction. Further, it is not the burden of Appellants to show that White does not disclose the direct update instruction.

With respect to independent claim 9, claim 9 recites the elements of “directly setting the flag register by a first instruction or setting the flag register to a data value obtained by a second instruction.” As mentioned above, the direct update instruction of claim 1 is an instruction that directly sets or clears a flag. Thus, the first instruction of claim 9 is equivalent to the direct update instruction of claim 1. Similarly, the indirect update instruction of claim 1 is an instruction that obtains data from the system data path and updates a flag value based upon that data. Thus, the second instruction of claim 9 is equivalent to the indirect update instruction of claim 1. Therefore, for the reasons mentioned above in regard to claim 1, White does not anticipate claim 9.

Claims 2, 3, 6-8, and 13-15 depend from claims 1 and 9, respectively, and incorporate the limitations thereof. Thus, for at least the reasons mentioned above in regard to claim 1, White does not anticipate these dependent claims.

Accordingly, Appellants request the Board to overturn the § 102 rejection of claims 1-3, 6-9, and 13-15.

### **C. Claims Rejected Under 35 U.S.C. § 103(a) Over White in View of Hennessy**

#### **1. Claims 4, 5, 10-12, and 20-22**

Claims 4, 5, 10-12, and 20-22 stand rejected under 35 USC § 103(a) as being allegedly unpatentable over White in view of Hennessy. Appellants submit that White in view of Hennessy does not teach or suggest each of the elements of these claims.

To establish a *prima facie* case of obviousness, the Examiner must show that the cited references, combined, teach or suggest each of the elements of a claim. In regard to claims 4, 5, 10-12 and 20-22, these claims depend from independent claims 1, 9 and 19, respectively, and incorporate the limitations thereof. As mentioned above in regard to claims 1 and 9, White fails to teach or suggest each of the elements of claims 1 and 9. With respect to independent claim 19, claim 19 includes many elements similar to those of claim 9. In the rejection of claim 19 as unpatentable over White, the Examiner offers the same basis for rejecting the claim as presented for claim 9. Thus, at least for the reasons mentioned above in regard to independent claim 9, White fails to teach or suggest each of the elements of claim 19.

Therefore, for at least the foregoing reasons, White fails to teach or suggest each of the elements of independent claims 1, 9, and 19. Further, Hennessy does not cure the defects of White. The Examiner has not relied upon and Appellants have been unable to discern any part of Hennessy that teaches or suggests the direct update instruction and indirect update instruction handling recited in the independent claims. Thus, White in view of Hennessy does not teach or suggest each of the elements of these claims.

Moreover, there is no motivation to combine White and Hennessy. The Examiner alleges that “it would have been obvious to one of ordinary skill in the art at the time of invention to have included Hennessy’s scoreboarding technique in White’s data processor for the benefit of ensuring register data is valid before operating on it.” However, the reorder buffer of White and the scoreboarding of Hennessy are two different techniques for solving the same technical problem, namely, out-of-order executions. White uses a reorder buffer to store instruction results and the destination register numbers. The reorder buffer thus enforces data dependencies and ensures the validity of register data before the register data is operated on (see col. 4, lines 21-58

and, generally, col. 34-col. 35). The scoreboarding technique of Hennessy uses a table (i.e., a scoreboard) to record the status of pending instructions and register results (page 247, FIG. 4.4). Thus, the scoreboard of Hennessy also enforces data dependencies and ensures the validity of register data before the register data is operated on. Neither reference describes any advantage if the two techniques were to be combined. Thus, a person of ordinary skill in the art would not be motivated to combine White with Hennessy for achieving the same result, because the combination would result in redundant hardware that would unnecessarily increase hardware complexity and therefore cost without any benefit. See MPEP § 2143.01 I. The Prior Art Must Suggest the Desirability of the Claimed Invention.

Accordingly, Appellants request the Board to overturn the § 103 rejection of claims 4, 5, 10-12 and 20-22.

#### **D. Claims Rejected Under 35 U.S.C. § 103(a) Over White**

##### **1. Claims 16-19 and 23-28**

Claims 16-19 and 23-28 stand rejected under 35 U.S.C. § 103 as being allegedly unpatentable over White.

Claim 19 includes many elements similar to those of claim 9. Further, the Examiner offers the same basis for rejecting the claim as presented for claim 9. Thus, at least for the reasons mentioned above in regard to independent claim 9, White fails to teach or suggest each of the elements of claim 19.

Claims 16-18 and 23-28 depend from independent claims 9 and 19, respectively, and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to

independent claims 9 and 19, White fails to teach or suggest each of the elements of these claims.

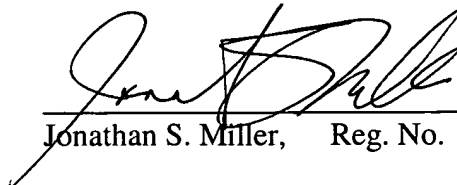
Accordingly, Appellants request the Board to overturn the § 103 rejection of claims 16-18 and 23-28.

Based on the foregoing, the Board should overturn the rejection of all pending claims and hold that all of the claims currently pending in the application under review are allowable.

Respectfully submitted,

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Dated: 10/11, 2006

  
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|                                                                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                              |
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| <p>12400 Wilshire Boulevard<br/>Seventh Floor<br/>Los Angeles, California 90025<br/><br/>(310) 207-3800</p> | <p style="text-align: center;"><b><u>CERTIFICATE OF MAILING</u></b></p> <p>I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:<br/>Commissioner for Patents<br/>Alexandria, VA 22313-1450</p> <p> 10/11/06<br/>Amber D. Saunders Date</p> |
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## VIII. CLAIMS APPENDIX

The claims involved in this appeal are presented below.

1. (Original) A method comprising:  
  
setting a flag for a processor via a first instruction, the first instruction being either a  
  
direct update instruction or an indirect update instruction;  
  
if the setting of the flag is by a direct update instruction, executing a succeeding second  
  
instruction that reads the flag prior to completion of the first instruction; and  
  
if the setting of the flag is by an indirect update instruction, delaying the second  
  
instruction until after completion of the first instruction.
2. (Original) The method of claim 1, wherein setting the flag by a direct update instruction  
comprises storing a value for the flag in a renamer.
3. (Original) The method of claim 2, wherein setting the flag by an indirect update  
instruction comprises storing a value in a buffer and storing the value in the renamer  
upon retirement of the indirect update instruction.
4. (Original) The method of claim 3, further comprising checking the value of a register  
scoreboard prior to accessing the flag.
5. (Original) The method of claim 4, wherein executing an indirect update instruction  
comprises setting the register scoreboard prior to storing the value in the renamer and  
clearing the register scoreboard after storing the value in the renamer.

6. (Original) The method of claim 1, further comprising storing the value for the flag in shadow logic.
7. (Original) The method of claim 6, wherein the shadow logic is enabled if the value was provided by a direct update instruction.
8. (Previously Presented) The method of claim 7, wherein the shadow logic is disabled if the value was not provided by a direct update instruction.
9. (Previously Presented) A processor comprising:
  - an execution unit to execute instructions; and
  - a renamer, the renamer to rename a flag register and store the value for the flag register; the value of the flag register being set by one of a plurality of processes, the processes
    - including directly setting the flag register by a first instruction or setting the flag register to a data value obtained by a second instruction; and
  - a succeeding third instruction being executed without being stalled if the value of the flag register was set by the first instruction and being stalled until conclusion of the second instruction if the value of the flag register is set by the second instruction.
10. (Original) The processor of claim 9, further comprising a scoreboard register, the first instruction and the second instruction checking the scoreboard register before setting the flag register.
11. (Original) The processor of claim 10, wherein the first instruction and the second instruction delay storage of the flag register if the scoreboard register is enabled.

12. (Original) The processor of claim 11, wherein execution of the second instruction includes setting the scoreboard register before setting the flag register and clearing the scoreboard register after setting the flag register.
13. (Original) The processor of claim 9, further comprising shadow logic to store values for the flag register.
14. (Original) The processor of claim 13, wherein the shadow logic includes a validity register to indicate validity of stored values for the flag register.
15. (Original) The processor of claim 14, wherein the validity register is enabled if a value for the flag register is provided by the first instruction and the validity register is disabled if the value for the flag register is provided by the second instruction.
16. (Original) The processor of claim 9, wherein the flag register is one of an interrupt flag or a direction flag.
17. (Original) The processor of claim 16, wherein the first instruction is an instruction to set or clear the flag register.
18. (Original) The processor of claim 9, wherein the second instruction is an instruction to pop a data value from a memory stack.
19. (Previous Presented) A system comprising:
  - a bus;
  - a flash memory coupled to the bus; and
  - a processor coupled to the bus, the processor comprising:

an execution unit to execute instructions; and

a renamer, the renamer to rename a flag register and store the value for the flag register;

the value of the flag register being set by one of a plurality of processes, the processes

including directly setting the flag register by a first instruction or setting the flag register to a data value obtained by a second instruction; and

a succeeding third instruction being executed without being stalled if the value of the flag register was set by the first instruction and being stalled until conclusion of the second instruction if the value of the flag register is set by the second instruction.

20. (Original) The system of claim 19, wherein the processor further comprises a scoreboard register, the first instruction and the second instruction checking the scoreboard register before setting the flag register.
21. (Original) The system of claim 20, wherein the first instruction and the second instruction delay storage of the flag register if the scoreboard register is enabled.
22. (Original) The system of claim 21, wherein execution of the second instruction includes setting the scoreboard register before setting the flag register and clearing the scoreboard register after setting the flag register.
23. (Original) The system of claim 19, wherein the processor further comprises shadow logic to store values for the flag register.
24. (Original) The system of claim 23, wherein the shadow logic includes a validity register to indicate validity of stored values for the flag register.

25. (Original) The system of claim 24, wherein the validity register is enabled if a value for the flag register is provided by the first instruction and the validity register is disabled if the value for the flag register is provided by the second instruction.
26. (Original) The system of claim 19, wherein the flag register is one of an interrupt flag or a direction flag.
27. (Original) The system of claim 26, wherein the first instruction is an instruction to set or clear the flag register.
28. (Original) The system of claim 19, wherein the second instruction is an instruction to pop a data value from a memory stack.

## **IX. EVIDENCE APPENDIX**

No evidence is submitted with this appeal brief.

## **X. RELATED PROCEEDINGS APPENDIX**

No related proceedings exist.